WHAT IS CLAIMED IS:

1. A digital to analog converter, comprising:

a noise shaping modulator for modulating an input digital data stream;

a plurality of output elements for generating a plurality of intermediate data streams from a modulated output stream from the modulator;

an output summer for summing the intermediate data streams to generate an output analog stream; and

wherein the noise shaping modulator balances an edge transition rate of the output elements such that the edge transition rate of two selected elements is approximately equal.

2. The data converter of Claim 1, wherein the plurality of output elements comprises at least eight output elements.

3. The digital-to-analog converter of Claim 1, wherein the modulator balances a duty cycle of the output elements, such that the usage of two selected elements is approximately equal.

4. A data converter, comprising:

a duty cycle modulator for converting a received data stream having a frequency into a duty cycle modulated data stream; and

a finite impulse response filter for filtering harmonics of the frequency of the received data stream from the duty cycle modulated data stream.

5. The data converter of Claim 4, wherein the finite impulse response filter has a null at a repeat rate of the duty cycle modulated data stream.

6. The data converter of Claim 4, further comprising a plurality of digital to analog conversion elements coupled to corresponding taps of the finite impulse response filter.

7. The data converter of Claim 6, wherein the plurality of digital to analog conversion elements comprise continuous time conversion elements.

8. The data converter of Claim 7, wherein the conversion elements comprise controlled current sources.

9. The data converter of Claim 7, wherein the conversion elements comprise resistors.

10. The data converter of Claim 4, further comprising:

a second duty cycle modulator for converting a second data stream having a frequency into a second duty cycle modulated data stream; and

a second finite impulse response filter for filtering harmonics of the frequency of the second data stream from the second duty cycle modulated data stream.

11. The data converter of Claim 10, further comprising combining circuitry for combining outputs of the first and second filters.

12. The data converter of Claim 10, further comprising de-interleaving circuitry for de-interleaving an input data stream into the received data stream and the second data stream.

13. The data converter of Claim 12, further comprising a delta-sigma modulator for noise shaping the input data stream, wherein the delta-sigma modulator has a noise transfer function with multiple attenuation bands for reducing noise exposure to mismatch between the duty cycle modulator and the second duty cycle modulator.

14. The data converter of Claim 4, wherein the received data stream is generated by a delta-sigma modulator having at least one integrator and non-linear feedback to the at least one integrator.

15. The data converter of Claim 14, wherein the non-linear feedback corrects for variations in a selected moment of the duty cycle modulated data stream.

16. The data converter of Claim 15, wherein the non-linear feedback is provided by a selected one of non-linear feedback operations.

17. A digital to analog converter, comprising:

a noise shaper for generating a noise-shaped data stream at a first frequency;

at least one pulse width modulator stage for generating from the noise-shaped data stream a pulse width encoded data stream at a second frequency of a selected multiple of the first frequency;

output circuitry for converting the pulse width encoded data stream into an analog signal comprising:

a finite impulse response filter for filtering the pulse width encoded data stream at a frequency greater than or equal to the second frequency; and

a plurality of digital to analog conversion elements coupled to selected taps of the finite impulse response filter for generating an output analog signal.

18. The digital to analog converter of Claim 17, wherein the noise shaper comprises a delta-sigma modulator having a plurality of integration stages and correction circuitry for selectively feeding back correction factors to selected ones of the integration stages for correcting for variations in a moment of the pulse width encoded stream.

19. The digital to analog converter of Claim 17, wherein the at least one pulse width modulation stage comprises a plurality of parallel pulse width modulation stages, wherein the digital to analog converter further de-interleaves the noise shaped data stream into a plurality of data streams corresponding to the plurality of pulse width modulation stages and each of the plurality of data streams has a frequency proportional to the frequency of the noise shaped data stream and a number of the plurality of pulse width modulation stages.

20. The digital to analog converter of Claim 19, wherein the noise shaper comprises a delta-sigma modulator with multiple noise attenuation bands in an output noise transfer function for reducing noise exposure to mismatch between the plurality of pulse width modulation stages.

21. The digital to analog converter of Claim 17, wherein the plurality of digital to analog conversion elements comprises a plurality of continuous-time digital to analog conversion elements.

22. A delta-sigma data converter, comprising:

a delta-sigma modulator for quantizing received data into first and second quantized samples; and

first and second interleaved output elements respectively operating on the first and second quantized samples to generate first and second output streams with balanced transition densities.

23. The delta-sigma modulator of Claim 22, wherein the delta-sigma modulator has a multiple attenuation band transfer function selected to balance mismatch between the first and second interleaved continuous time output elements.

24. The delta-sigma data converter of Claim 22, further comprising first and second interleaved pulse width modulators for converting the first and second quantized samples into first and second pulse width modulated signals for respectively driving the first and second interleaved output elements.

25. The delta-sigma data converter of Claim 22, further comprising a digital filter system having taps driving the first and second output elements.

26. The delta-sigma data converter of Claim 22, wherein the first and second output elements comprise continuous-time one-bit digital to analog conversion elements having outputs summing to generate the output signal.

27. A method of data conversion, comprising:

converting a data stream having a frequency into a duty cycle modulated data stream; and

filtering harmonics of the frequency of data stream from the duty cycle modulated data stream with a finite impulse response filter.

28. The method of Claim 27, further comprising noise shaping the data stream at the frequency prior to conversion into the duty cycle modulated data stream at a higher slot frequency.

29. The method of Claim 28, wherein filtering harmonics further comprises filtering the stream of duty cycle modulated data patterns at a frequency equal or greater to the slot frequency.

30. A data converter, comprising:

first and second noise shapers interleaved in time to noise shape corresponding portions of a stream of input data; and

first and second finite impulse response filters respectively filtering output data streams from the first and second noise shapers.

31. The data converter of Claim 30, further comprising first and second sets of digital to analog conversion elements coupled to corresponding taps of the first and second finite impulse response filters.

32. The data converter of Claim 30, wherein the first and second finite impulse response filters further comprise digital-in, analog-out finite impulse response filters.

33. The data converter of Claim 30, wherein the digital to analog conversion elements further comprise continuous-time conversion elements.

34. A data converter comprising a signal input, a first and second duty cycle modulated signals responsive to the input signal, a first controllable current source responsive to the first duty cycle signal, a second controllable current source responsive to the second duty cycle signal, and a summer responsive to both controlled current sources.